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CASE HISTORY—PEER-REVIEWED

Failure Analysis on Blind Vias of PCB for Novel Mobile Phones

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Abstract Failure of blind via is one of the main causes of an open circuit in printed circuit boards (PCBs). By using macroscopic and microscopic testing methods and characterization techniques, the failure analysis of the vias on PCB for novel mobile phones has been systematically carried out. Metallographic inspection shows obvious cracking along the interface of different copper layers. Micrograph observation and chemical analysis on the grain boundary have definitely identified that inappropriate location of the vias concerned with circuit design and residue sulfur related to incomplete desmear process predominantly account for cracking of blind vias, and the occurrence of the cracking is caused by the formation of a brittle Cu_xS layer. Moreover, the influence of warpage on the reliability of the via was noted. Based on these defaults, improvement countermeasures and suggestions are addressed in the paper and are of significant value for reference to the safe reliability and structural integrity of PCB products during manufacturing and services.

Keywords Blind via · Cracking · Sulfur embrittlement · PCB · Failure analysis

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Introduction

With the expansion of high-density interconnection (HDI) in electronic packaging technology, blind via is a newly developed type of microvia, providing electrical interconnection among different laminates of a printed circuit board (PCB). Blind vias comprise electroless copper on top of buried interconnects formed from various kinds of copper foil and underneath subsequent coatings of electroplated copper. Blind vias can be constructed by laser ablating the holes in the top layer of the board material. Holes formed are then cleaned and a layer of electroless copper deposited in the hole, followed by coatings of electroplated copper on top of that layer [1]. Therefore, inappropriate circuit and geometry design, improper manufacturing process, and poor plating quality can directly affect yield and electrical reliability of PCB. An open circuit is one of the frequent faults that occur during manufacturing [2].

Blind vias play a crucial role in HDI packaging technology because of their desirable electrical performance and low reflection. However, it is critical to evaluate the reliability of these structures. The technologies for manufacturing blind vias have been addressed [3, 4]. The thermomechanical reliability of them is usually evaluated theoretically by experimental tests such as FEM simulation and impact tests etc. [5–8]. However, comprehensive analyses on failure of blind vias after actual services have rarely been reported. Marks [9] introduced several practical failure cases of flip-chip packaging, but skipped the research on blind vias. Also, the chemical mechanism for the cracking generation in the vias has not been well studied.

Based on our former study on failure ball grid array (BGA) solder joints [10], further analysis on blind vias of the two types of PCB was carried out. Since visual inspection is the first and important step in failure

investigation [11], a series of modern analytical instruments and methods such as stereomicroscope, optical microscope (OM), and digital microscope (3D) were used to observe the failure. The scanning electron microscope (SEM), energy dispersive spectroscopy (EDS), and focus ion beam (FIB) were adopted to reveal the cracking morphologies and chemical compositions of the vias. Characterization techniques such as Fourier transform infrared spectroscopy (FT-IR), thermogravimetric analyses (TGA), and scanning acoustic microscopy (SAM) were also used to inspect the bare board. The cracking mechanism and the causes of the failure were definitely revealed. Preventive countermeasures and suggestions are given in this paper.

Brief Introduction of the Failed PCBs

Figure 1 shows the circuit configuration of both sides with components on two types of PCBs, respectively, with dimension of $92 \times 37 \times 1.1$ mm for type 1 and $81 \times 38 \times 0.98$ mm for type 2. Open-circuit faults have been detected mainly around BGA solder joints and solder bars of several components and chips by automatic optical inspection (AOI). The faults induce failure of the whole board. During macroscopic inspection, circuit configurations of components on type 1 PCB are not distorted, but obvious warpage has been found in type 2 PCB. Modern analytic instruments and characterization methods have been adopted in order to find the primary causes.

Characterization and Microstructural Observation

The results of FT-IR (Fig. 2) show that the two types of PCB have an FR-4 flame-resistant substrate and that the raw materials are all bromized epoxy resin. TGA curves in Fig. 3 indicate that the materials reach their thermal decomposition temperature (T_d) at about 323 °C. The T_d of bromized epoxy resin is generally above 300 °C, and the soldering peak temperature in surface mounting technology (SMT) of PCB is below 270 °C. Therefore, the raw materials can endure the instantaneous high temperature and the failure should have no relationship to the soldering processes.

Microscopic study was carried out at low magnification using stereomicroscope and at higher magnification using OM and 3D. Figures 4 and 5, respectively, present the morphologies of the failure blind vias on both types of PCBs. From Fig. 4(c) and (d), distinct cracking can be seen between the copper plating layer and the pad of the blind via. As illustrated in Fig. 4(b), the pad is not located right in the center of the via. Consequently, a strong thermal stress will occur around part of the via, leading to an asymmetric thermal deformation under conditions of reflow soldering or service. Moreover, the mismatch of coefficient of thermal expansion (CTE) between the plating layer and copper foil will enhance the thermal stress, finally resulting in the fracture from one side of the via. The location of the blind via in Fig. 5 indicates that the via and the BGA solder pad are too close to each other, just like the case shown in Fig. 4. An obvious microvoid in the copper foil, in which there appeared to be some debris, and an apparent crack in the bottom of the via, are displayed in Fig. 5(c) and (d).

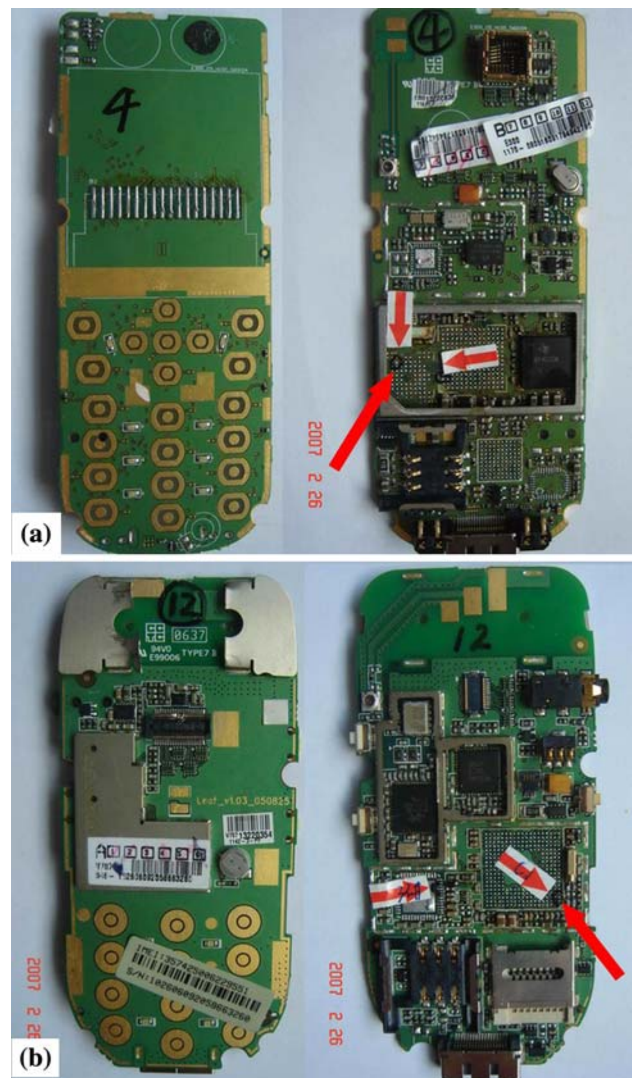


Fig. 1 Circuit configuration with components on PCBs. (**a**) Front and back face of Type 1 PCB. (**b**) Front and back face of Type 2 PCB

Cracking morphologies of the blind vias were further observed by SEM, and chemical compositions along the fracture line were analyzed by EDS in Figs. 6 and 7. A FIB was used to etch part of the surface of the deposited copper, and the microstructure near cracking is presented in Fig. 8.

SAM with a sensor of 100 MHz was used to detect delamination of the PCB before and after the thermal

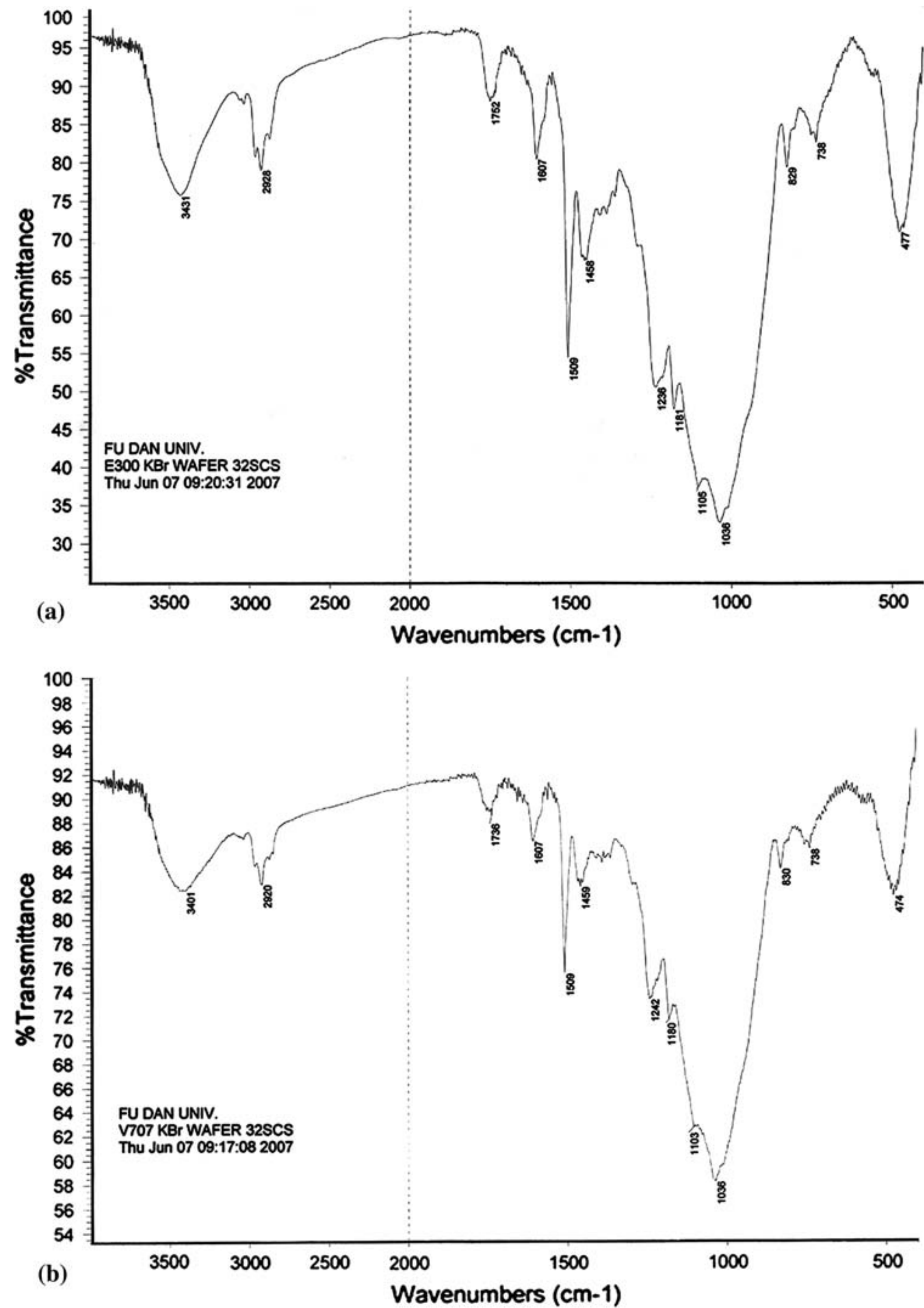


Fig. 2 FT-IR spectra of bare board. (**a**) Type 1. (**b**) Type 2

fatigue simulation testing to determine whether delamination influenced the reliability of resin-coated copper (RCC) foil. Testing conditions and parameters are listed in Table 1, and the delamination comparison of the bare board before and after the test is presented in Fig. 9. The results show that there is only a slight increase in the display of delamination on the whole board after the test and there is almost no noticeable delamination around the failure sections. Therefore, the open circuit is not caused by delamination.

Results and Discussion

The primary faults of these two types of PCBs are open circuits and the resistance deviating from the standard value. The results of chemical compositions and thermal analysis show that the material quality of the bare board is acceptable. Meanwhile, the component configuration of type 1 PCB is reasonable, but warpage has been found in type 2 PCB through the macroscopic inspection. It can be concluded from the SAM inspection that delamination is not the

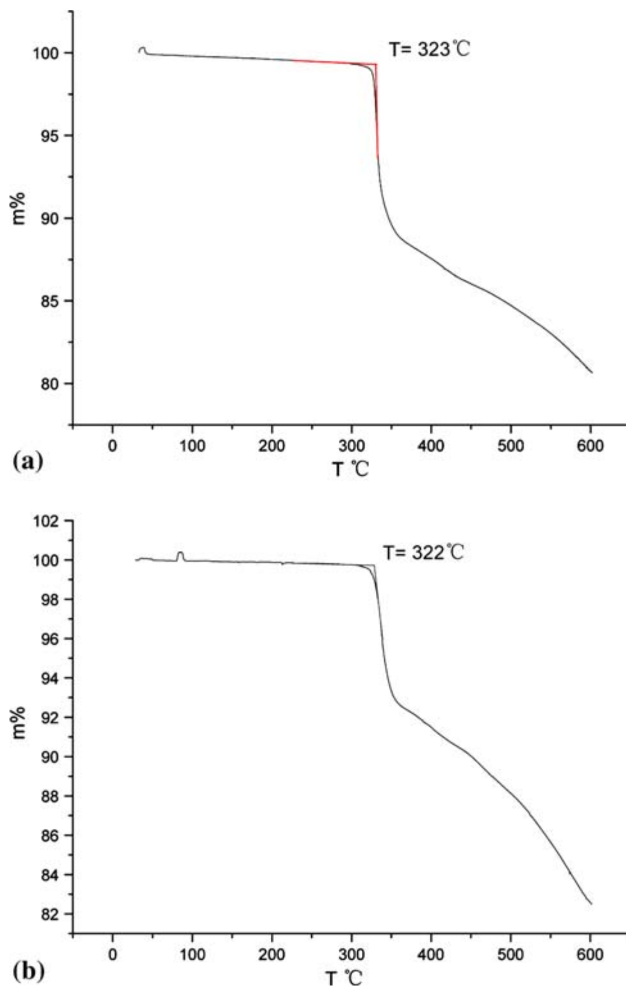


Fig. 3 TGA curve of bare board. (**a**) Type 1. (**b**) Type 2

main cause of failure. The analytical results show that it is the defect of the blind vias that leads to the open circuits.

A big open cracking from one side of the blind via with a result of a separation completely between the pad and the copper-plating layer is shown in Fig. 6. An obvious cracking from the bottom of the other blind via that partly separated the via and the copper foil is presented in Fig. 7. We can also notice from the location of these two blind vias that the design position between pads and blind vias is somewhat improper. They are not kept in the same Z-direction, and the distance between them is too small. Usually, the region close packed with deep color dots shows a comparatively faster rate of heating. Therefore, temperature around the pads covered with solder of dark color rises faster than pad areas without solder during the heating for reflow soldering; while temperature in the areas with just the pads drops faster than in those overlaid with solder in the cooling segment of reflow soldering. The mismatch CTE of these two areas results in a strong thermal stress and an asymmetric deformation in the blind vias linked closely to the pad uncovered with solder. Accordingly, the improper circuit design regarding the location of blind vias and pads is the leading cause of vias cracking.

In addition, the EDS results (Fig. 6c and 7c) demonstrate that a certain amount of sulfur which usually leads to embrittlement concentrates at the interface. Higher magnifications of the cracking and many microcracks can be seen in Fig. 7(d)–(g). These microcracks are generated along the deposited copper grains. Microstructure of the grains near cracking has also been obtained by FIB, with a sound characteristic of intercrystalline fracture. It can be

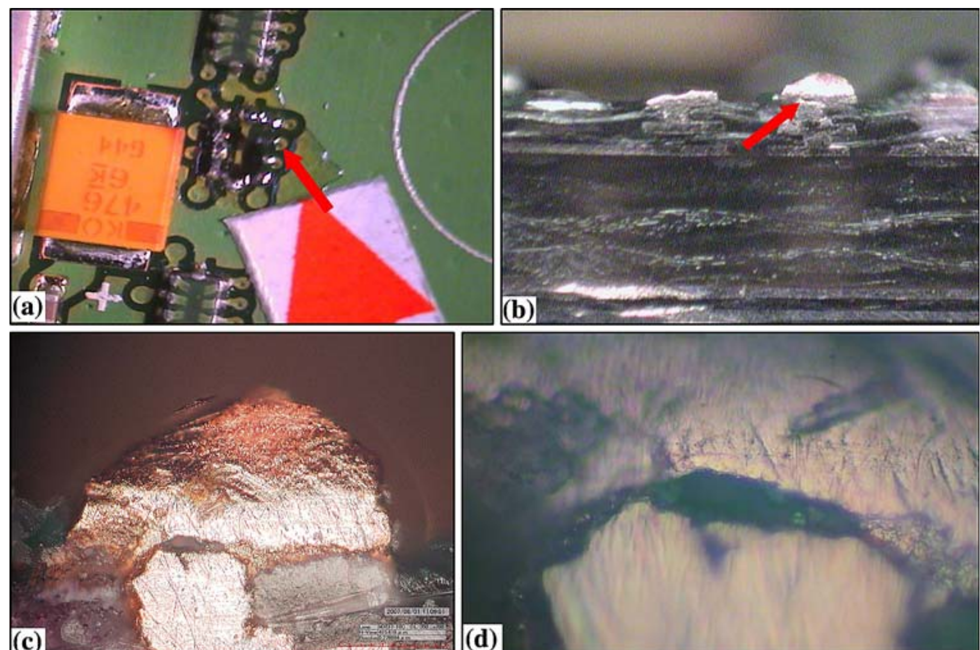


Fig.4 (**a**) Location of the failure blind via (type 1). (**b**) Appearance of the via. 4.5× (**c**) and (**d**) Cracking morphologies by 3D and OM. 40× and 60×

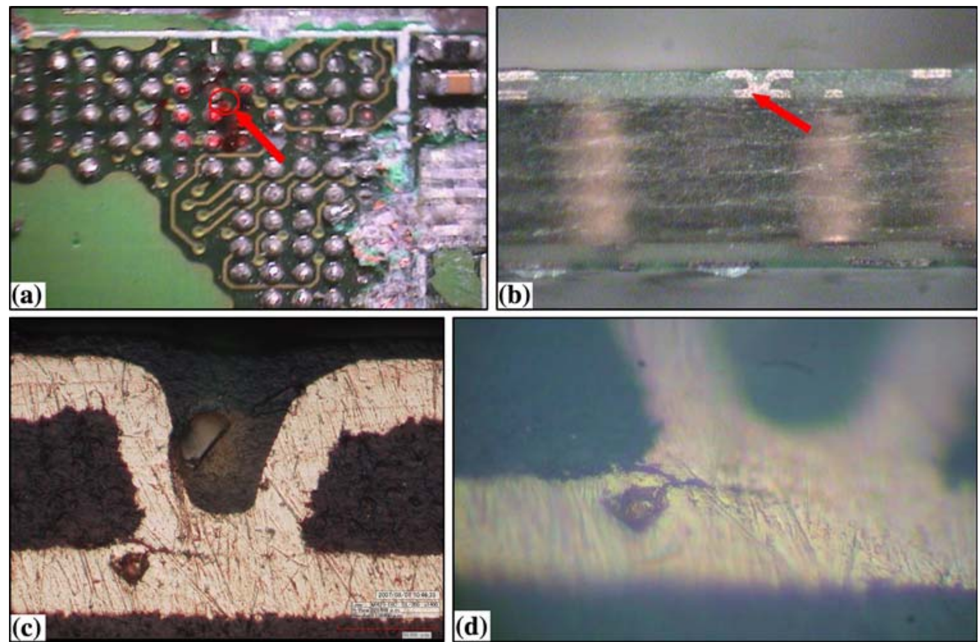


Fig. 5 (**a**) Location of the failure blind via (type 2). (**b**) Appearance of the via 4.5×. (**c**) and (**d**) Cracking morphologies by 3D and OM. 40× and 60×

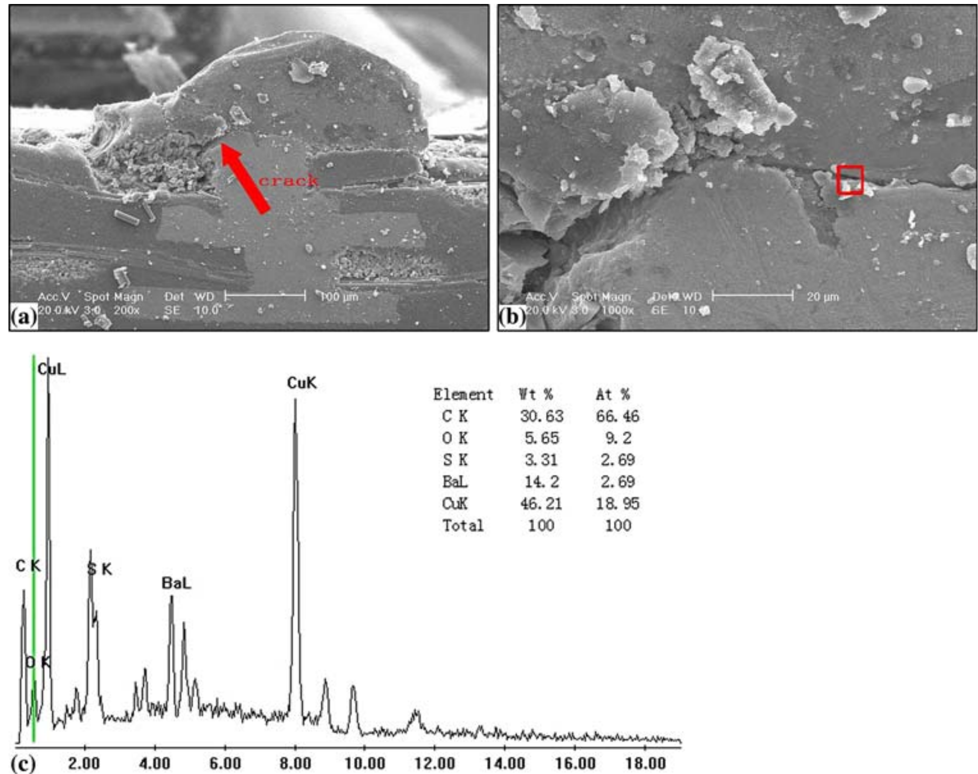


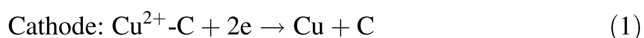
Fig. 6 SEM-EDS results of the failure blind via. (**a**) SEM micrograph of blind via. (**b**) Morphology of the cracking. (**c**) EDS analysis of the element compositions in the crack

deduced that the S impurity in the crack has a deleterious effect on the blind via and lowers the bonding force among different layers.

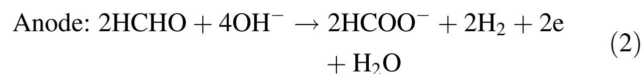
From the process viewpoint, the blind vias are plated with several layers of copper after the drilling and desmear procedures to produce electrical conductivity on the surface of fiberglass and resins. As a result, the reliability of the vias may also be influenced by the process and quality of plating. Electroless plating solutions generally contain copper sulfate, complex agent, reducing agent, pH conditioning agent, and additives with S and N, and so forth. A layer of copper is deposited on the wall of the blind via through a self-catalyzed oxidation-reduction reaction.

During electroless plating, complex copper ions (Cu^{2+}-C) obtain electrons that are directly provided by reducing agent and then turn into Cu.

Fig. 7 SEM-EDS results of the failure blind via. (**a**) and (**b**) SEM micrographs of the via. (**c**) EDS analysis of the element compositions in the crack. (**d**)–(**g**) Morphologies of the cracking

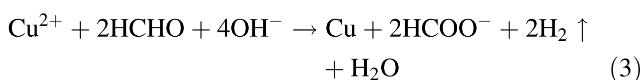


$$\text{Cathode: } Cu^{2+}\text{-C} + 2e \rightarrow Cu + C \quad (1)$$



$$\text{Anode: } 2HCHO + 4OH^- \rightarrow 2HCOO^- + 2H_2 + 2e + H_2O \quad (2)$$

The entire reaction is listed as:



$$Cu^{2+} + 2HCHO + 4OH^- \rightarrow Cu + 2HCOO^- + 2H_2\uparrow + H_2O \quad (3)$$

The acquisition of pure copper is, however, difficult because of the tendency for intergranular segregation of sulfur and subsequent embrittlement. The defect in the structure of copper grain boundaries is such that precipitation of sulfur is favored as the sulfur weakens the boundaries. Fractures in the vias were observed preferentially at grain boundaries [12].

The morphologies of the cracks of the blind vias exhibit obvious embrittlement deformation behaviors in the fractured copper-plating layer. Generally speaking, the S content in pure copper, calculated in weight percentage (wt.%), is not more than 0.005 to 0.01%. However, the content of S impurity detected in the fracture interface by

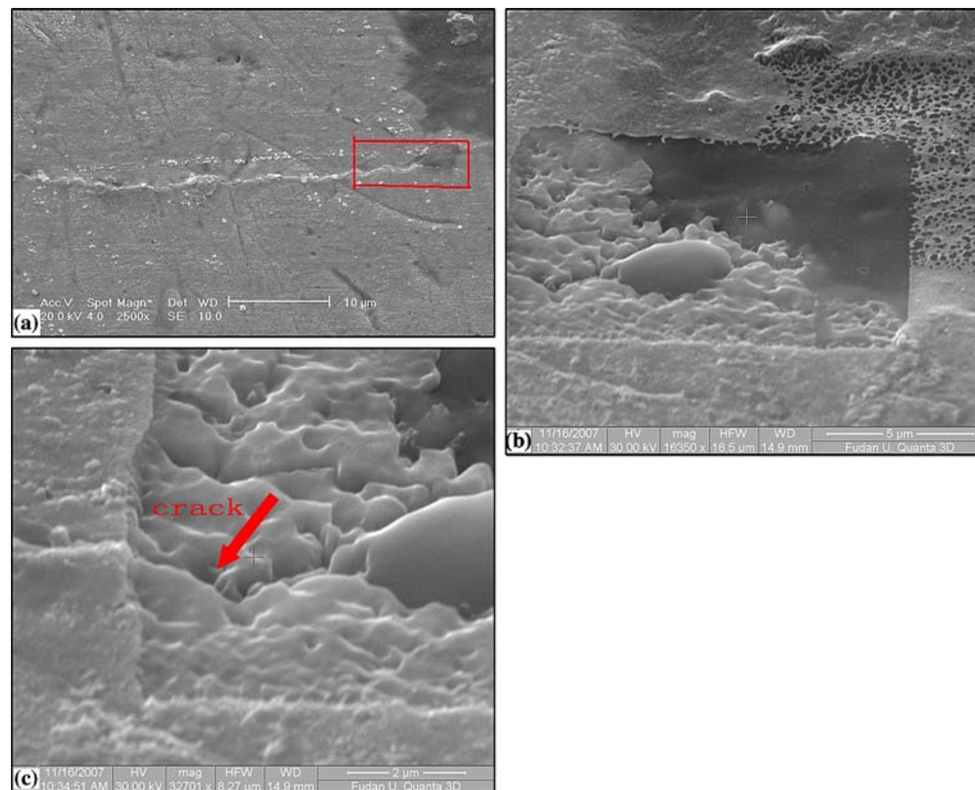


Fig. 8 FIB microstructure. (**a**) Etching section. (**b**) and (**c**) Morphologies of the cracking

Table 1 Conditions of thermal cycle testing on the bare board

Range of cycle temperature, C	−40–125
Heat-up cycle, min	13 (up) + 20 (remaining)
Cool-down cycle, min	17 (down) + 20 (remaining)
Times for thermal cycle	200

EDS is far above the standard, as is shown in the former part. Thus, it can be assumed that this embrittlement fracture is largely affected by segregation of S at grain boundary.

Although the structure formed by the segregated S at grain boundaries is still unknown, the formation of Cu_xS compounds can be expected, especially Cu_2S. Similar evidence was also found by Boulliard and Sotto [13] that the structure of segregated sulfur on the face of Cu (100) single crystals was 8 S atoms on 17 Cu atoms, with the S atoms arranged in a p(2 × 2) lattice. Note that this coverage approximates the stoichiometry of Cu_2S phase, which is highly stable [14]. It was also reported that the phase transition from the "high chalcocite" hexagonal phase to the complex "low chalcocite" phase occurs at 103.5 °C for $x = 2.000$, but drops to 90 °C for the slightly more sulfur-rich compound with $x = 1.990$.

Hence, the mechanism of the cracking generation in the blind vias occurs through the following steps. The sulfur segregated to the surface along the different layers of the vias probably nucleated as a set of three-dimensional islands of Cu_xS, which would be expected to grow until they coalesced. The nucleation sites may be at dislocation or grain-boundary intersections with the surface [15]. This is highly undesirable, and there are several structural transformations of Cu_xS in the temperature interval of interest. These transformations favor the fatal crack nucleation and propagation at grain boundaries under the thermal stress generated during reflow soldering. Consequently, the conclusion can be reached that the residue of S impurity along copper grain boundary has a significant influence on the reliability of the blind vias, which is the predominant cause of the failure. The residue S primarily results from the desmear process and the cleaning of the blind vias.

Moreover, through macroscopic observation, apparent warpage can be noticed in type 2 PCB with a discrepancy of about 1 mm between the right and left sides of the board. As mentioned previously, the type 2 PCB is only 0.98 mm thick, the thickness of which is at least 10% thinner than that of type 1 PCB. It is both the improper reduction of the thickness and asymmetric configuration of components on the board that lead to the excessive warpage and deformation of the board, which will produce a big tensile force or a bending stress around pads linked

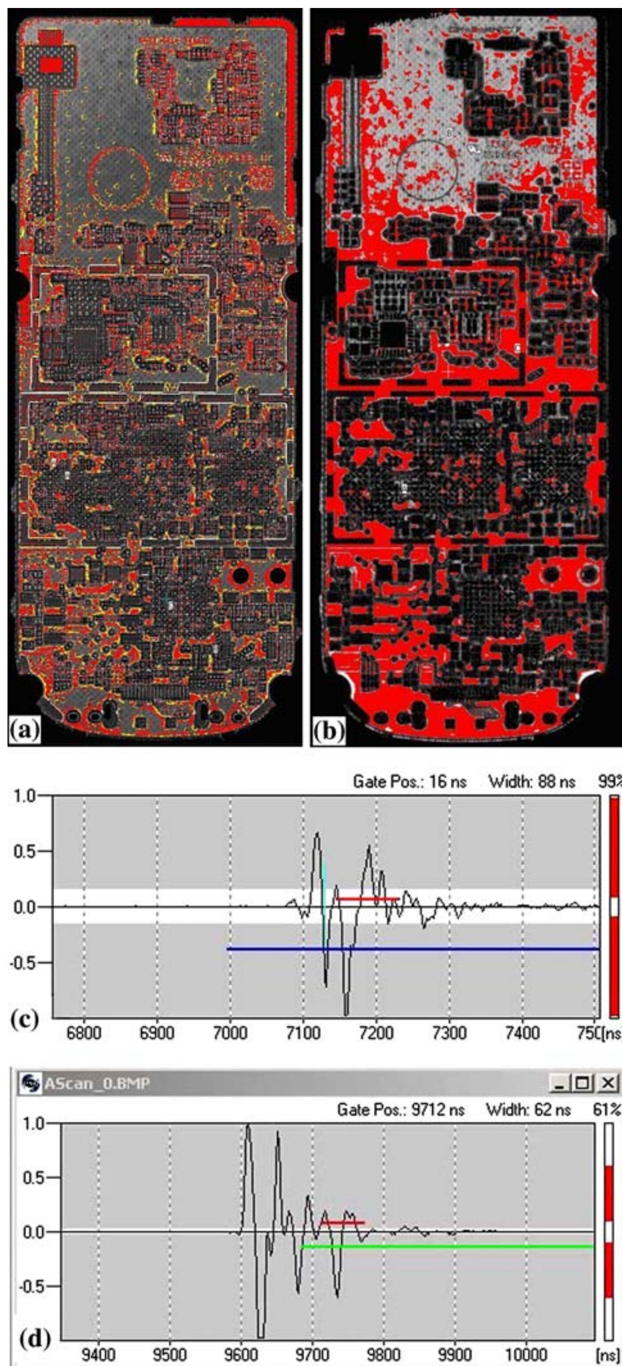


Fig. 9 SAM inspection of the bare board before and after thermal cycle test. (**a**) Before testing. (**b**) After testing. (**c**) Spectra before testing. (**d**) Spectra after testing

with blind vias, leading to a cracking in some weak connections of different layers in the vias.

In summary, both the improper location design of pads and blind vias and the incomplete desmear process before copper plating constitute the main causes of the cracking. The inappropriate dimension design of type 2 PCB is another potential risk of failure.

Conclusions

- The comprehensive analysis on the two types of PCBs by both macroscopic and microscopic methods shows that cracking of the blind vias causes open-circuit faults in the PCBs. The raw materials of the boards are acceptable, and there is also no noticeable delamination around the failure sections.
- Improper locations of pads and blind vias are based on improper circuit design, and lead to high stresses and asymmetry deformations that generate cracking in some weak joints once heated. Therefore, the design default is a primary cause for cracking of the blind vias.
- The residue S appearing in the wall interface of the blind vias has a fatal effect on the structural integrity and deposition quality of the copper plating with a formation of Cu_xS in the interface of copper grains. The structure of Cu_xS can change with different temperatures, inducing an embrittlement intercrystalline fracture during SMT. Accordingly, the incomplete desmear is the predominant factor for failure of the vias.
- An inappropriate reduction in thickness of type 2 PCB and together with the asymmetric configuration of components lead to excessive warpage and deformation of the board, which will generate a big tensile force or a bending stress around pads linked with blind vias. However, under some conditions, cracking will occur in those weak connections of the vias. So, the unsuitable dimension design of the PCB is another potential risk of failure.

Suggestions

- It is advised that the design of relative locations among pads and components should be optimized through simulation testing including finite element methods (FEM) and bench test.
- Meanwhile, the quality inspection on the wall of the blind vias should be emphasized before plating to provide a clean wall surface.
- The best thickness of the board should be simulated through FEM and essential property experiments to ensure adequate stiffness of the substrate.

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